Please type a plus sign (+) inside this box [+] 01-03-00

A

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 042390.P8228 Total Pages 3

First Named Inventor or Application Identifier Andrew W. Martwick

Express Mail Label No. EL 431 887 405 US

ADDRESS TO:	**Assistant Commissioner for Patents** **Box Patent Application** **Washington, D. C. 20231**

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. [X] Specification (Total Pages 14)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. [X] Drawings(s) (35 USC 113) (Total Sheets 3)

4. [X] Oath or Declaration (Total Pages 5)
   a. [ ] Newly Executed (Original or Copy)
   b. [ ] Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. [ ] DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. [ ] Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program (Appendix)

7. [ ] Nucleotide and/or Amino Acid Sequence Submission

(if applicable, all necessary)

a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)

_X_ b. Power of Attorney

10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449

_____ b. Copies of IDS Citations

12. _____ Preliminary Amendment
13. _X_ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)

b. Statement filed in prior application, Status still proper and desired

15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. _X_ Other: Certificate of Express Mail with copy of postcard showing contents of Express Mail package.

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

___ Continuation ____ Divisional ____ Continuation-in-part (CIP)

of prior application No: _____

18. **Correspondence Address**

_____ Customer Number or Bar Code Label _____ (Insert Customer No. or Attach Bar Code Label here)

or

_X_ Correspondence Address Below

NAME John P. Ward Reg No.: 40,216

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

ADDRESS 12400 Wilshire Boulevard

Seventh Floor

CITY Los Angeles STATE California ZIP CODE 90025-1026

Country U.S.A. TELEPHONE (408) 720-8598 FAX (408) 720-9397

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

EXPRESS MAIL CERTIFICATE OF MAILING

"Express Mail" mailing label number: EL431887405US
Date of Deposit: December 30, 1999
I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Lisa Kaiser
(Typed or printed name of person mailing paper or fee)

Lisa Kaiser
(Signature of person mailing paper or fee)

12/30/99
(Date signed)

Serial/Patent No.: *** Filing/Issue Date: ***
Client: Intel Corporation
Title: Integrated System Management Memory For System Management Interrupt Handler Independent Of Bios And Operating System.
BSTZ File No.: 042390.P3
Date Mailed: December 30, 1999
Atty/Secty Initials: IPW/CKW/lyk
Docket Due Date: ***

The following has been received by the U.S. Patent & Trademark Office on the date stamped hereon:

- ☐ Amendment/Response (____ pgs.)
- ☐ Appeal Brief (____ pgs.) (in triplicate)
- ■ Application - Utility (14 pgs., with claims)
- ☐ Application - Rule 1.53(b) Continuation (____ pgs.)
- ☐ Application - Rule 1.53(b) Divisional (____ pgs.)
- ☐ Application - Rule 1.53(b) CIP (____ pgs.)
- ☐ Application - Rule 1.53(d) CPA Transmittal (____ pgs.)
- ☐ Application - Design (____ pgs.)
- ☐ Application - PCT (____ pgs.)
- ☐ Application - Provisional (____ pgs.)
- ☐ Assignment and Cover Sheet
- ☐ Certificate of Mailing
- ■ Declaration & POA (5 pgs.) (unsigned)
- ☐ Disclosure Docs & Ltr & Copy of Invents Signed Letter (____ pgs)
- ■ Drawings: 3 # of sheets includes 3 figures

- ■ Check No. 32541 Amt: $ 690.00
- ☐ Check No. _____ Amt: _____
- ■ Small Entity Statement(s) (Filed)
- ☐ Information Disclosure Statement & PTO 1449 (____ pgs.)
- ☐ Issue Fee Transmittal
- ☐ Notice of Appeal
- ☐ Petition for Extension of Time
- ☐ Petition for _____
- ■ Postcard
- ☐ Power of Attorney (____ pgs)
- ☐ Preliminary Amendment (____ pgs.)
- ☐ Reply Brief (____ pgs.)
- ☐ Response to Notice of Missing Parts
- ☐ Small Entity Declaration for Indep. Inventor/Small Business
- ■ Transmittal Letter, in duplicate
- ■ Fee Transmittal, in duplicate

■ Other: Certificate of Express Mail with copy of postcard showing contents of Express Mail package.

Attorney Docket No. 42390.P8228

APPLICATION FOR UNITED STATES PATENT

FOR

INTEGRATED SYSTEM MANAGEMENT MEMORY FOR SYSTEM MANAGEMENT INTERRUPT HANDLER INDEPENDENT OF BIOS AND OPERATING SYSTEM

Inventors: Andrew W. Martwick

Prepared by: Blakely, Sokoloff, Taylor & Zafman
12400 Wilshire Blvd. 7th Floor
Los Angeles, CA 90025-1026
(408) 720-8598

"Express Mail" mailing label number: EL 431 887 405 US
Date of Deposit: December 30, 1999
I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Lisa Kaiser
(Typed or printed name of person mailing paper or fee)

Lisa Kaiser
(Signature of person mailing paper or fee)

December 30, 1999
(Date signed)

INTEGRATED SYSTEM MANAGEMENT MEMORY FOR SYSTEM MANAGEMENT INTERRUPT HANDLER INDEPENDENT OF BIOS AND OPERATING SYSTEM

Field Of The Invention

The present invention pertains to the field of computer systems. More particularly, this invention pertains to the field of integrating a system management memory into a memory controller for a system management interrupt handler that is independent of both BIOS and operating system.

Background of the Invention

A large majority of today's personal computer systems implement a system management interrupt (SMI). An SMI signal is asserted to a processor to alert the processor that an SMI event has occurred. The SMI signal is typically asserted to the processor by a system logic device that includes a memory controller. The system logic device may assert the SMI signal for any of a large number of possible reasons. For example, the SMI signal may be asserted if a system resource seeks access to a certain range of memory or to a particular input/output address. These memory and input/output addresses can be programmable via a set of registers that typically reside in the system logic device. The SMI signal may also be asserted if certain system events occur. For example, a computer system may be implemented with a variety of timers for timing a variety of system events. The SMI signal may be asserted if any of these timers expire.

An assertion of the SMI signal indicates to the processor that the processor should begin to fetch instructions from an address stored in one of the processor's registers. This register is sometimes referred to as the system management memory base address register. The memory space located at the address indicated by the system management

memory base address register may be referred to as system management memory (SMM). The SMM has stored therein an SMI handler routine. The SMI handler may be implemented to perform any of a wide variety of functions. For example, the SMI handler may perform power management functions, or may try to correct system malfunctions.

The SMM, and therefore the SMI handler, is under control of the computer system's Basic Input/Output System (BIOS). The BIOS is typically designed and implemented by one of several BIOS software companies. The SMI handler is typically installed in the computer system during the system manufacturing process.

Often, there is a need to make changes to the SMI handler after the manufacturing process. One such situation can occur when a chipset manufacturer desires to provide a solution for an erratum or desires to either enable new features or disable old features. These desires can be met by altering the SMI handler. However, a chipset manufacturer's product may be utilized in computer systems built by dozens of different computer system manufacturers. Further, these system manufacturers typically use any of a number of BIOS software companies to design and implement the SMI handler. Therefore, if the chipset manufacturer needs to have the SMI handlers modified, it must negotiate with many different parties to have the changes made. The chipset manufacturer may also try to negotiate with operating system vendors to have the operating systems implement the chipset manufacturer's requests. Neither of these alternatives is desirable, in larger part to the large amount of time and effort required to perform the negotiations and to implement the chipset manufacturer's requests.

Brief Description of the Drawings

The invention will be understood more fully from the detailed description given below and from the accompanying drawings of embodiments of the invention which, however, should not be taken to limit the invention to the specific embodiments described, but are for explanation and understanding only.

Figure 1 is a block diagram of a computer system including one embodiment of a memory controller implemented in accordance with the invention.

Figure 2 is a flow diagram of an embodiment of a method for utilizing an integrated system management memory region.

Figure 3 is a flow diagram of an embodiment of an additional method for utilizing a system management memory integrated into a memory controller.

Detailed Description

An embodiment of a memory controller with an integrated system management memory region will be described. The memory controller receives an SMI acknowledge signal from a processor. The processor then delivers a system management memory address to the memory controller. Instead of fetching SMI handler instructions from the address indicated by the processor, the memory controller instead fetches SMI handler instructions from its integrated system management memory region. At the end of the integrated system management memory's SMI handler, the processor is instructed to fetch instructions from the address originally specified by the processor. In this manner, a BIOS SMI routine may be executed after the integrated SMI routine is executed. The integrated system management memory region allows chipset or other system component manufacturers to distribute proprietary SMI routines without the need to involve BIOS or operating system vendors. The proprietary SMI routines may be utilized for any purpose that can be accomplished via a software routine, including, but not limited to, providing solutions for errata or enabling or disabling system or chipset features.

Figure 1 is a block diagram of a computer system 100 that includes a processor 110 coupled to a memory controller 120. The system 100 also includes a system main memory 150 that is also coupled to the memory controller 120.

The memory controller 120 includes a host interface unit 122 that facilitates communication with the processor 110. When an SMI event occurs, the host unit asserts a system management interrupt signal 111 to the processor 110. Systems may be implemented with a wide variety of SMI events, including, but not limited to, power management functions and accesses to particular regions of memory. The term "SMI

event" as used herein is meant to include a broad range of computer system activities that computer system designers may wish to implement as activities that trigger the execution of a system management interrupt handler routine.

After the processor 110 receives the system management interrupt signal 111, the processor returns a system management interrupt acknowledge signal 113 to the memory controller 120. The processor 110 also delivers a fetch address to the memory controller via a host bus 115. The fetch address delivered by the processor 110 corresponds to an address stored in a system management memory base address register in the processor (not shown). The address stored in the system management memory base address register indicates where in memory space BIOS system management memory resides.

The fetch address delivered by the processor 110 over the host bus 115 is latched by a latch 134 that is located in a system management interrupt address decode unit 130. The fetch address is delivered to the latch 134 via an address path 121 that couples the host unit 122 with other units in the memory controller 120. Once the fetch address is latched in the latch 134, a set signal 131 is delivered to a flip-flop 135. The set signal 131 causes an select signal 137 to be asserted. The select signal 137 indicates to a decoder 132 to fetch the SMI handler routine from a system management memory 124 that is integrated into the memory controller 120. The decoder fetches SMI handler instructions from the system management memory 124, and the instructions are delivered to the processor 110. The processor 110 executes the delivered SMI handler instructions.

The SMI handler routine stored in the system management memory 124 includes at the conclusion of the routine an instruction that tells the processor 110 to jump to the address stored in the latch 134. A compare unit 136 receives addresses delivered by the

processor 110 to the host interface unit 122 over the address path 121. The compare unit 136 compares the received addresses with the contents of the latch 134. A match between a newly received address and the contents of the latch 134 indicates that the SMI routine stored in the system management memory 124 has been completely executed and that the processor 110 is now attempting to access the SMI routine stored at the address originally specified in the processor's system management memory base address register. When a match is found, the compare unit 136 delivers a reset signal 133 to the flip-flop 135. The reset signal 133 results in the select signal 137 being deasserted. The decoder 132 will then fetch instructions from the SMM space pointed to by the matched address.

The SMM space originally pointed to by the address stored in the processor's system management memory base address register may reside in a BIOS system management memory space 152 that is located in the system main memory 150. The decoder 132 accesses the BIOS system management memory space 152 via a system main memory interface 126.

The status of a BIOS SMI enable register 138 determines whether the SMI routine stored in BIOS system management memory space 152 will be executed following the execution of the SMI routine stored in the system management memory 124. The BIOS SMI enable register 138 communicates its status to the decoder 132 via an enable signal 139.

Another embodiment of the memory controller 130 may include an enable register that when cleared would prevent the integrated SMI routine from executing. Setting this register would allow the integrated SMI handler routine to execute as described above.

Figure 2 is a flow diagram of a method for executing an SMI handler routine stored in an integrated system management memory. At step 210, a system management interrupt acknowledge signal is received from a processor. At step 220, system management interrupt handler instructions are fetched from a system management memory integrated into a memory controller. The instruction fetch from the integrated system management memory is in response to the receipt of the system management interrupt acknowledge signal at step 210.

Figure 3 is a flow diagram of an additional embodiment of a method for executing an SMI handler stored in a system management memory integrated into a memory controller. At step 310, a system management interrupt acknowledge signal is received from a processor. Following step 310, a system management memory address delivered by the processor is latched at step 320. A system management interrupt handler instruction is then fetched from an integrated system management memory at step 330. The fetch is from the integrated memory regardless of what address was specified by the processor. At step 340 the processor executes the fetched instruction.

At step 350 a compare operation is performed to determine whether an address newly delivered by the processor matches the address previously latched at step 320. If the addresses do not match, then the process flow returns to step 330. If, however, the addresses do match, then at step 360 a system management interrupt handler is fetched from a BIOS controlled area of system main memory.

Although the example embodiments described above discuss the system management memory region as being integrated into a memory controller, other embodiments are possible with the system management memory region located

elsewhere. Having a system management memory region that is physically separate from the BIOS controlled system management memory region and also separate from system main memory has a benefit in that neither the BIOS nor any other operating system or program can inadvertently overwrite the system management memory.

In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than in a restrictive sense.

CLAIMS

What is claimed is:

1. An apparatus, comprising:

an integrated system management memory region; and

a system management interrupt address decode unit to fetch instructions from the integrated system management memory region in response to a system management interrupt acknowledge signal asserted by a processor, the system management interrupt decode unit to fetch instructions from the integrated system management memory region regardless of a system management interrupt address received from the processor.

2. The apparatus of claim 1, the system management interrupt address decode unit to latch the system management interrupt address received from the processor.

3. The apparatus of claim 2, wherein the system management interrupt address is the first address received following the assertion of the system management interrupt acknowledge signal by the processor.

4. The apparatus of claim 3, wherein the system management interrupt address decode unit includes a compare unit to compare a plurality of addresses received from the processor with the latched system management interrupt address.

5. The apparatus of claim 4, the system management interrupt address decode unit to fetch system management interrupt handler instructions stored in a system main memory in response to the compare unit finding a match between the latched system management interrupt address and one of the plurality of addresses received from the processor.

6. The apparatus of claim 5, wherein the system management interrupt handler instructions stored in the system main memory are part of a basis input/output system (BIOS).

7. The apparatus of claim 6, wherein the integrated system management memory region is at least 128 bytes in size.

8. A method, comprising:

receiving a system management interrupt acknowledge signal from a processor; and

fetching a plurality of system management interrupt handler instructions from an integrated system management memory in a memory controller in response to the system management interrupt acknowledge signal.

9. The method of claim 8, wherein fetching a plurality of system management interrupt handler instructions from an integrated system management memory includes fetching the system management interrupt handler instructions from the integrated system management memory regardless of a system management memory address indicated by the processor.

10. The method of claim 9, further comprising latching the system management memory address indicated by the processor.

11. The method of claim 10, wherein latching the system management memory address includes latching a first address delivered by the processor following receiving the system management interrupt acknowledge signal.

12. The method of claim 11, further comprising comparing a plurality of addresses received from the processor with the latched address.

13. The method of claim 12, further comprising fetching a plurality of system management interrupt handler instructions from a section of BIOS code in a system main memory if comparing a plurality of addresses received from the processor with the latched address results in a match.

14. A system, comprising:

a processor;

a system main memory; and

a memory controller coupled between the processor and the system main memory, the memory controller including

an integrated system management memory region, and

a system management interrupt address decode unit to fetch instructions from the integrated system management memory region in response to a system management interrupt acknowledge signal asserted by the processor, the system management interrupt decode unit to fetch instructions from the integrated system management memory region regardless of a system management interrupt address received from the processor.

15. The system of claim 14, the system management interrupt address decode unit to latch the system management interrupt address received from the processor.

16. The system of claim 15, wherein the system management interrupt address is the first address received by the memory controller following the assertion of the system management interrupt acknowledge signal by the processor.

17. The system of claim 16, wherein the system management interrupt address decode unit includes a compare unit to compare a plurality of addresses received from the processor with the latched system management interrupt address.

18. The system of claim 17, the system management interrupt address decode unit to fetch system management interrupt handler instructions stored in the system main memory in response to the compare unit finding a match between the latched system management interrupt address and one of the plurality of addresses received from the processor.

19. The system of claim 18, wherein the system management interrupt handler instructions stored in the system main memory are part of a basis input/output system (BIOS).

20. The system of claim 19, wherein the integrated system management memory region is at least 128 bytes in size.

ABSTRACT OF THE DISCLOSURE

A memory controller with an integrated system management memory region is disclosed. The memory controller receives an SMI acknowledge signal from a processor. The processor then delivers a system management memory address to the memory controller. Instead of fetching SMI handler instructions from the address indicated by the processor, the memory controller instead fetches SMI handler instructions from its integrated system management memory region. At the end of the integrated system management memory's SMI handler, the processor is instructed to fetch instructions from the address originally specified by the processor. In this manner, a BIOS SMI routine may be executed after the integrated SMI routine is executed.

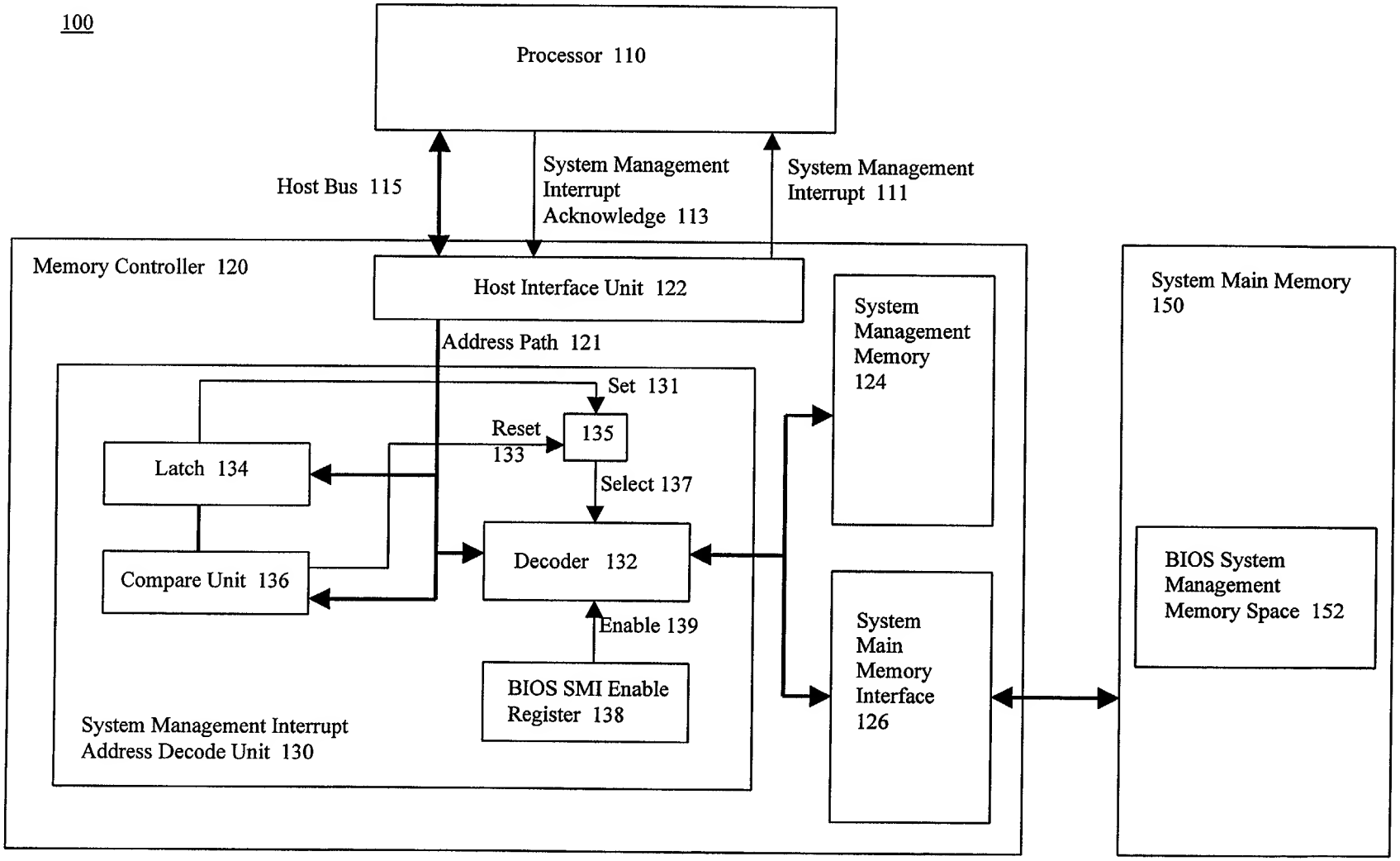
100
Processor 110
Host Bus 115
System Management Interrupt Acknowledge 113
System Management Interrupt 111
Memory Controller 120
Host Interface Unit 122
Address Path 121
Set 131
Reset 133
135
Latch 134
Select 137
Compare Unit 136
Decoder 132
Enable 139
BIOS SMI Enable Register 138
System Management Interrupt Address Decode Unit 130
System Management Memory 124
System Main Memory 150
BIOS System Management Memory Space 152
System Main Memory Interface 126

Figure 1

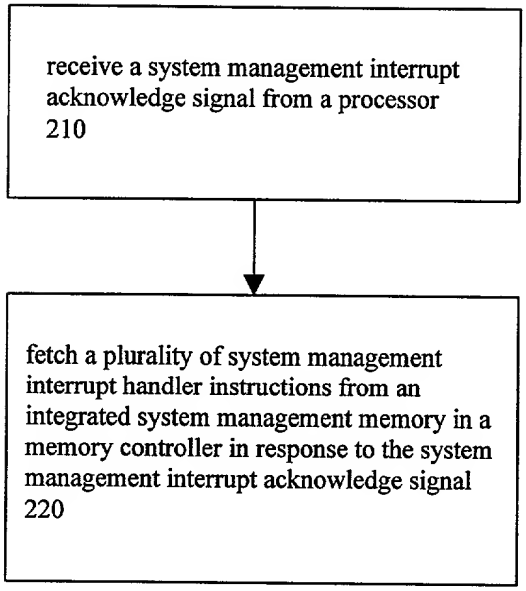
receive a system management interrupt acknowledge signal from a processor
210
fetch a plurality of system management interrupt handler instructions from an integrated system management memory in a memory controller in response to the system management interrupt acknowledge signal
220

Figure 2

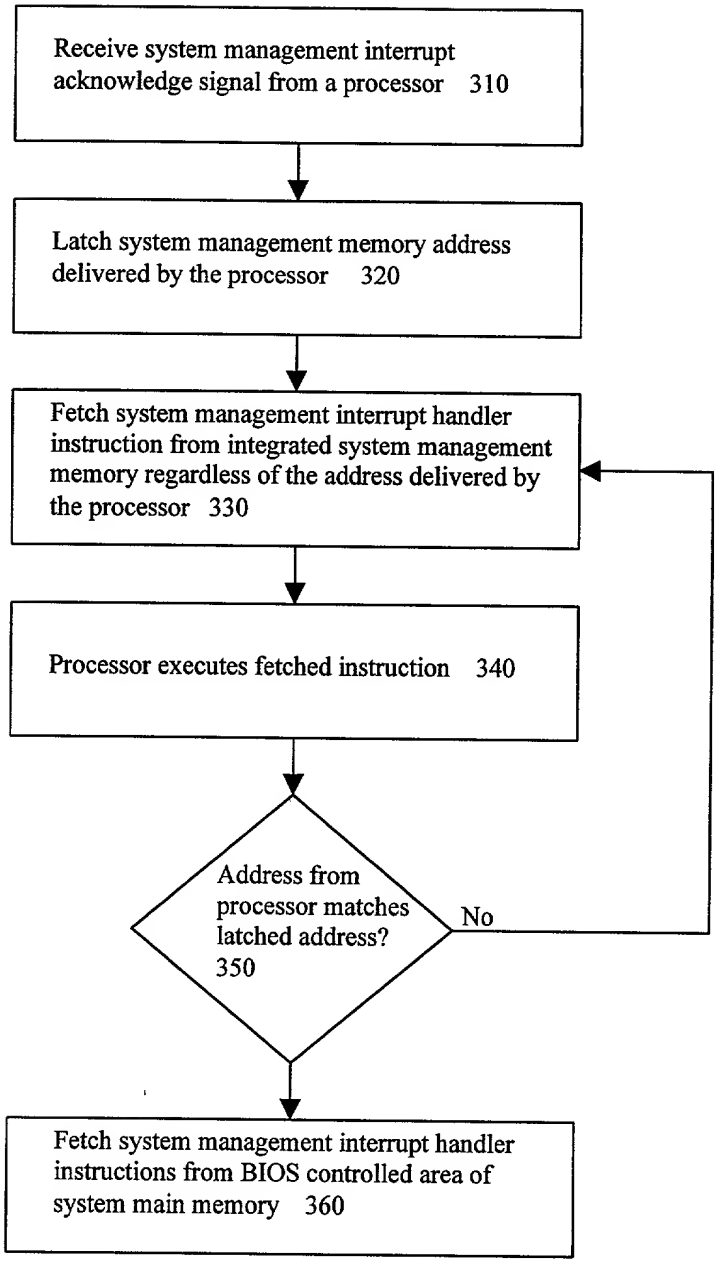
Receive system management interrupt acknowledge signal from a processor 310
Latch system management memory address delivered by the processor 320
Fetch system management interrupt handler instruction from integrated system management memory regardless of the address delivered by the processor 330
Processor executes fetched instruction 340
Address from processor matches latched address? 350
No
Fetch system management interrupt handler instructions from BIOS controlled area of system main memory 360

Figure 3

Attorney's Docket No.: 042390.P8228 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
Integrated System Management Memory For System Management Interrupt Handler Independent Of Bios And Operating System.

the specification of which

X is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to John P. Ward **(Name of Attorney or Agent), BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to** John P. Ward **(Name of Attorney or Agent), (408) 720-8598.**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Andrew W. Martwick

Inventor's Signature _____ Date _____

Residence Folsom, California (City, State) Citizenship USA (Country)

Post Office Address 9837 Oakplace West
Folsom, California 95630

William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Ronald C. Card, Reg. No. P44,587; Thomas M. Coester, Reg. No. 39,637; Stephen M. De Klerk, under 37 C.F.R. § 10.9(b); Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. P41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Erica W. Kuo, Reg. No. 42,775; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. 42,004; Lisa A. Norris, Reg. No. P44,976; Chun M. Ng, Reg. No. 36,878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Kimberley G. Nobles, Reg. No. 38,255; Daniel E. Ovanezian, Reg. No. 41,236; Babak Redjaian, Reg. No. 42,096; William F. Ryann, Reg. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey Sam Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; John F. Travis, Reg. No. 43,203; George G. C. Tseng, Reg. No. 41,355; Joseph A. Twarowski, Reg. No. 42,191; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Charles T. J. Weigell, Reg. No. 43,398; Kirk D. Williams, Reg. No. 42,229; James M. Wu, Reg. No. P45,241; Steven D. Yates, Reg. No. 42,242; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and Andrew C. Chen, Reg. No. 43,544; Justin M. Dillon, Reg. No. 42,486; Paramita Ghosh, Reg. No. 42,806; and Sang Hui Kim, Reg. No. 40,450; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Jeffrey S. Draeger, Reg. No. 41,000; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Charles A. Mirho, Reg. No. 41,199; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Kenneth M. Seddon, Reg. No. 43,105; Mark Seeley, Reg. No. 32,299; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells; Reg. No. P43,256, Peter Lam, Reg. No. P44,855; and Gene I. Su, Reg. No. 45,140; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.